The schematics for the eZdsp™ F28335 can be found on the CD-ROM that accompanies this board. The schematics were drawn on ORCAD.

The schematics are correct for both the socketed and unsocketed version of the eZdsp™.

**WARNING !**
The TMS320F28335 supports +3.3V Input/Output levels which are NOT +5V tolerant. Connecting the eZdsp to a system with +5V Input/Output levels will damage the TMS320F28335. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent latchup conditions.

**Design Notes:**

1. The TMS320F28335 X1/CLKIN pin is +1.8 volt input. The clock input is buffered with a SN74LVC1G14 whose supply is +1.8 volts. This provides +3.3 volts to the +1.8 volt clock translation. Refer to sheet 4 of the schematics.
The TMS320F28335 EzDSP design is based on preliminary information (SPR#439 June 2007) for the TMS320F28335 device. This schematic is subject to change without notification. Spectrum Digital Inc. assumes no liability for applications assistance, customer product design or infringement of patents described herein.

SCHEMATIC CONTENTS

SHEET01 - TITLE PAGE
SHEET02 - TMS320F28335 DSP
SHEET03 - DSP DECOUPLING CAPS
SHEET04 - BOOT SWITCHES, OSC
SHEET05 - MEMORY
SHEET06 - I/O MUXING
SHEET07 - CAN, RS232
SHEET08 - EMIF EXPANSION
SHEET09 - I/O EXPANSION
SHEET10 - ANALOG EXPANSION
SHEET11 - JTAG
SHEET12 - POWER
SHEET13 - PLACEMENT TOP
SHEET14 - PLACEMENT BOTTOM

Spectrum Digital, Inc
These caps go with U8

Tie in one point on the Ground plane
WHEN CRYSTAL IS USED POPULATE C42 WITH 0 OHM RESISTOR

WHEN OSCILLATOR IS USED POPULATE R32 WITH 0 OHM RESISTOR

Branch to SCI, skip ACC CAL
Branch to SARAM, skip ACC CAL
Branch to Flash, skip ACC CAL
Branch to check boot mode
Jump to SARAM

Parallel XINTF boot
Parallel GPIO I/O boot
Jump to OTP
Jump to XINTF x32
Jump to XINTF x16
 McBSP-A boot
 mCAN-A boot
IIC-A boot
SPI-A boot
SCI-A boot
Jump to Flash
Switch | Position | Value | Function
--- | --- | --- | ---
SW2-1 | OFF | 1 | Select GPIO0,GPIO1,GPIO10,GPIO11 as expansion
SW2-1 | ON | 0 | Select GPIO0,GPIO10,GPIO10,GPIO11 as on board SCI/CAN A
SW2-2 | OFF | 1 | Disable Mux U22
SW2-2 | ON | 0 | Enable Mux U22
SW2-3 | OFF | 1 | Select GPIO0,GPIO10,GPIO10,GPIO11 as expansion
SW2-3 | ON | 0 | Select GPIO0,GPIO10,GPIO10,GPIO11 as on board SCI/CAN B
SW2-4 | OFF | 1 | Disable Mux U23
SW2-4 | ON | 0 | Enable Mux U23
SW2-5 | OFF | 1 | Write Protect I2C EEPROM
SW2-5 | ON | 0 | Enable Writes to I2C EEPROM
SW2-6 | OFF | 1 | I2C EEPROM lowest address is 1
SW2-6 | ON | 0 | I2C EEPROM lowest address is 0
Make a solder connection on JR5 to the appropriate power supply. Note, JR4 also can power domains so this jumper should be set accordingly.

TMS320F28335 supports 3.3V input/output levels which are NOT 5V tolerant. Connecting the eZdsp to a system with 5V input/output levels will damage the TMS320F28335. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent latchup conditions.

To of unused eZdsp compatible signals.
TMS320F28335 supports 3.3V input/output levels which are NOT 5V tolerant. Connecting the ezDsp to a system with 5V input/output levels will damage the TMS320F28335. If the ezDsp is connected to another target then the ezDsp must be powered up first and powered down last to prevent latchup conditions.
Connect ADCLO to AGND or to ADCLO of target system for proper ADC operation.

PLACE R6 AS CLOSE TO DSP AS POSSIBLE

AGND
ADCINA0 2
ADCINA1 2
ADCINA2 2
ADCINA3 2
ADCINA4 2
ADCINA5 2
ADCINB0 2
ADCINB1 2
ADCINB2 2
ADCINB3 2
ADCINB4 2
ADCINB5 2
ADCINB6 2
ADCINB7 2
ADCREFM 2
ADCREFP 2
ADCINA6 2
ADCINA7 2
ADCLO 2
XRSn is logical AND of PONRSnIN and emulator controlled reset. Power on default is PONRSnIN controls XRSn.

USBSEL - HIGH, SELECT USB EMULATION
USBSEL - LOW, SELECT XDS EMULATION

Locate near DSP TCK pin
Locate R7, R54, C70 at the DSP XRSn pin for best EMI/ESD noise immunity.

IF U13 IS INSTALLED THEN REMOVE R49 AND R48.